Design Consideration of Front Deep Trench Isolation (FDTI) in Small-pitch, Dual-Photodiode Pixels

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***Abstract*—**In CMOS image sensors, Front Deep Trench Isolation (FDTI) is a unique structure governing both the electrical performance as well as the optical properties of a given pixel. Considering its layout directly affect pixel performance of dual-photodiode, one needs to tailor FDTI layout and corresponding trade-off carefully. In this paper, we explored two distinct FDTI layouts of sub-micron dual-photodiode pixels and their impact on pixel characteristics with phenomenological models.

I. INTRODUCTION

A dual-photodiode pixel (Fig. 1), which has two distinct photodiodes (PDs) in a single pixel, has been widely adapted in CMOS image sensor industry since it allows us to get PDAF (Phase-Detection Auto-Focus) information from every pixel across the pixel array. Conventional dual-photodiode with BDTI (Backside Deep Trench Isolation) is formed by ion implantation, however, recent dual-photodiode with FDTI incorporates conformal doping on DTI surface, which leads to larger full well capacity [1]. Such conformal doping scheme has been extended in dual-photodiode pixels to form electrostatic potential barrier between left and right PDs by modifying DTI layout, as shown in Fig. 2 (the left-hand side one). This particular layout, denoted as type A, has been used widely in the industry [1][3], but it has its own limitation since smaller pixel needs larger amount of n-type dopant to ensure large enough FWC and this may lead to lower potential barrier between left and right PD. In this regard, one needs to consider alternative of type A, and therefore in this paper, we propose type B (Fig. 2) and evaluate both types and compare them in various aspects.

II. RESULTS AND DISCUSSIONS

In this section, we compare type A and B in terms of three different aspects: FWC (Full Well Capacity), CG (Conversion Gain), and peak QE. First, as shown in Figure 3a, the concept of L (Left) / R (Right) FWC and PD FWC is depicted. Only PD FWC only matters in a single PD pixel, however, large enough L/R FWC in dual PD pixel needs to be obtained as it dictates PDAF performance. We evaluated L/R FWC and PD FWC for both type A and B with a range of N-type doping concentration for PD and the results are shown in Fig. 3b. Interestingly, two types of DTI layout shows different behavior: In type B L/R FWC and PD FWC are correlated in a linear manner, on the other hand, type A shows saturated L/R FWC while PD FWC keeps increasing.

To understand such difference, we measured the electrostatic potential barrier between left and right PD with dedicated TEG (Test Element Group). Fig.4 describes the method of extracting potential barrier

between the left and right PD. We obtained two distinct photodiode C-V curves with different bias conditions (Config. 1 and Config. 2). It allows us to easily estimate the actual barrier height.

For a number of different photodiode designs, we correlated PD FWC vs. potential barrier: The corresponding results (See Fig. 5a) revealed that the potential barrier does decrease as we increase FWC, and type A turns out to respond in more sensitive way. This may be attributed to the different amount of p-type dopant in the inter-PD region: For type A, at the two dead ends of DTI layout, the dopants injected by conformal doping process spread into silicon as if it is a two-dimensional diffusion process from a point source and this leads to lower concentration of p-type dopant and subsequently become more susceptible for barrier lowering. Type B, on the other hand, have one such dead end so it could be more robust to barrier lowering. TCAD simulation (shown in Fig. 5b) also supports such difference regarding inter-PD potential barrier for type A and B.

Second, Fig. 6(a) and (b) shows that type B pixel requires shorter metal routing path for connecting FD nodes and smaller number of contacts landing on silicon, which is translated in to a lower parasitic capacitance of FD node. It is straightforward that this can be beneficial in terms of achieving higher conversion gain (Fig. 6c).

The negative aspect of type B pixel is its poorer optical characteristics, especially regarding its peak QE. Fig. 7 shows the peak QE of type B is considerably degraded compared to that of type A because of the QE loss by presence of polysilicon inside FDTI. We demonstrated that such a significant degradation can be partially recovered by introducing low-loss FDTI structure (oxide/poly silicon/oxide), as shown in Fig. 8 [1].

III. CONCLUSION

In this paper, we introduce two different types of DTI layout and check both pixels in terms of typical pixel performance. Type B pixel outperforms type A for FWC and CG, but type A shows superior peak QE. These results could provide a design consideration for implementing smaller dual-PD pixels in the future.

IV. REFERENCES

[1] T. Jung et.al., "A 1/1.57-inch 50Mpixel CMOS Image Sensor with 1.0μm All-Directional Dual Pixel by 0.5μm-Pitch Full-Depth Deep-Trench Isolation Technology," *2022 IEEE International Solid-State Circuits Conference (ISSCC)*.

[2] D. Kim et.al., "A 1/1.56-inch 50Mpixel CMOS Image Sensor with 0.5μm pitch Quad Photodiode Separated by Front Deep Trench Isolation," *2024 IEEE International Solid-State Circuits Conference (ISSCC)*.

[3] K. Zaitsu et.al., "A 2-Layer Transistor Pixel Stacked CMOS Image Sensor with Oxide-Based Full Trench Isolation for Large Full Well Capacity and High Quantum Efficiency," *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*.

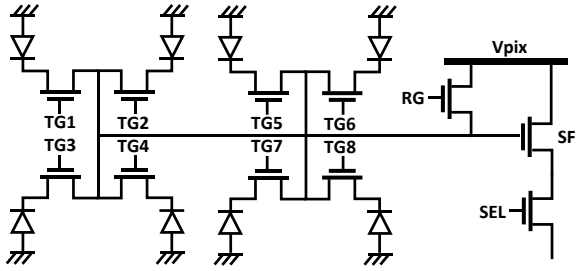

Figure 1. A schematic of four-shared, dual-photodiode pixels.

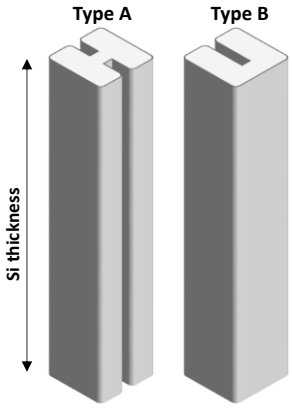

Figure 2. Illustration of DTI layouts: type A vs. B.

Figure 3. (a) Description of L/R FWC (Full Well Capacity) and PD FWC. (b) Correlation of L/R FWC vs. PD FWC (Si data).

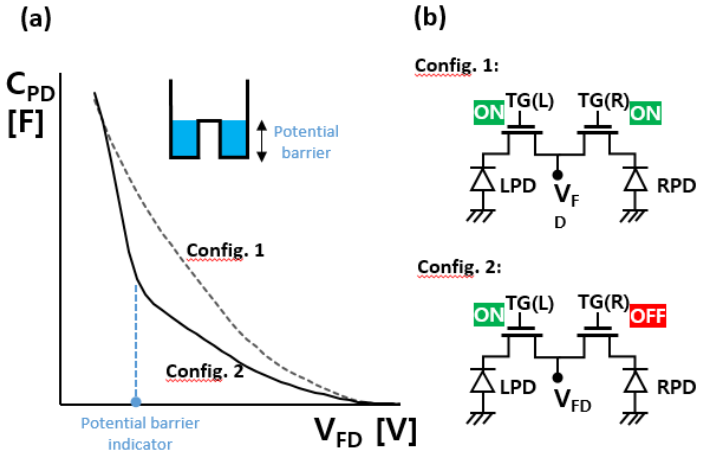

Figure 4. (a) Extraction method of the potential barrier between left/right PD measured in TEG (Test Element Group). (b) Illustration of bias condition for Config. 1 and Config. 2 shown in (a).

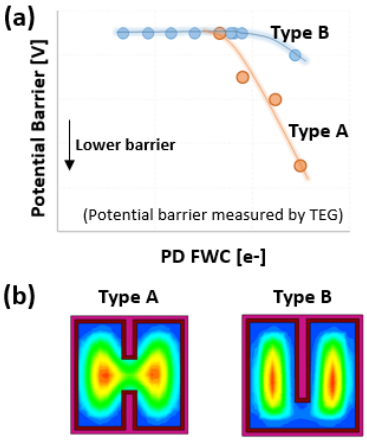

Figure 5. (a) Behavior of potential barrier between Left PD and right PD vs. PD FWC. (b) Electrostatic potential profile inside photodiode of type A and B (TCAD simulation).

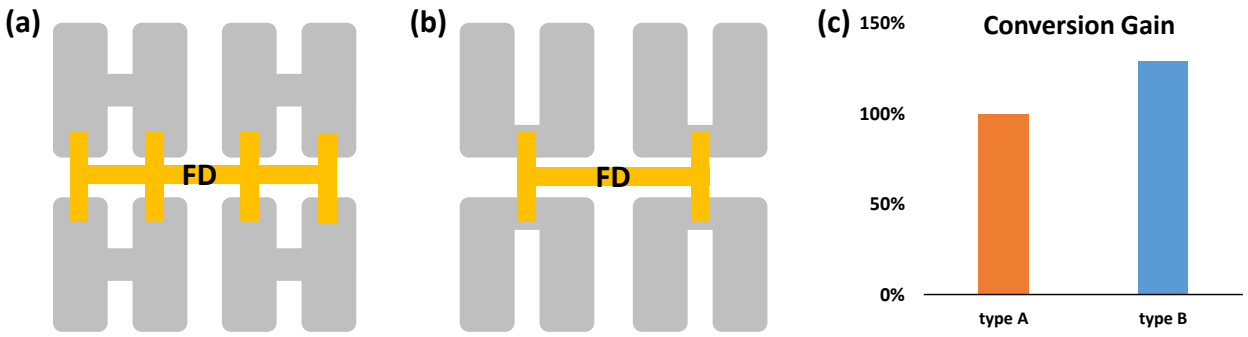

Figure 6. (a), (b) Local routing layout of type A and B. (c) Conversion gain comparison of type A and B (Si data).

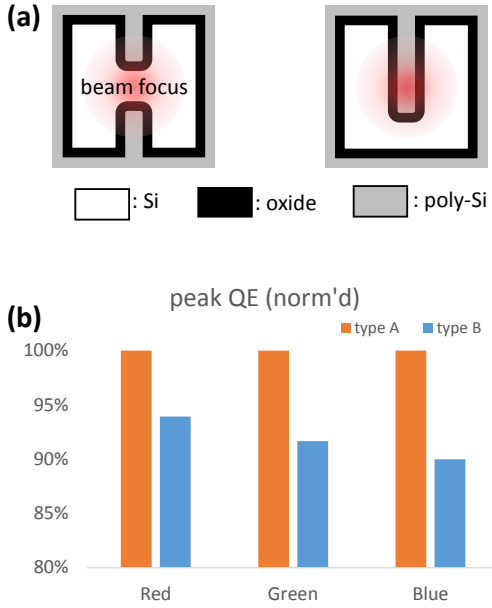

Figure 7. (a) Illustration of beam focus and (b) its peak QE for DTI filled with oxide-polysilicon layers (Si data).

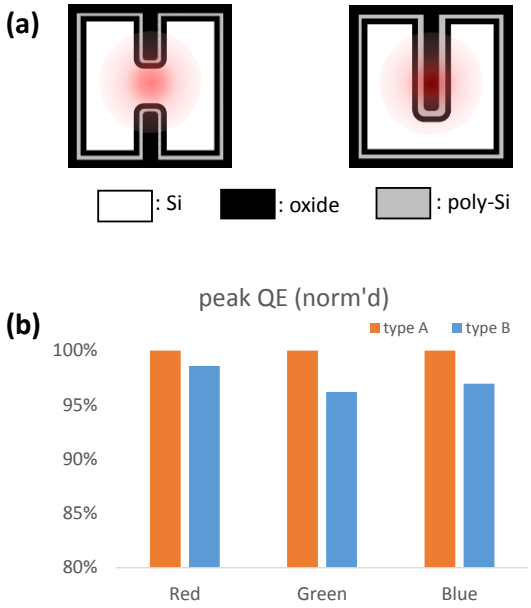

Figure 8. (a) Illustration of beam focus and (b) its peak QE for DTI filled with oxide-polysilicon-oxide layers (Si data).